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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,618	12/27/2001	Seung-Hwan Lee	P67474US0	9115

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,618	LEE ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 10/12/05 in which claims 1-8 are pending. The applicant's arguments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stott et al U.S. Patent No 6,320,917 B1 in view of Yamada et al US Pub NO 2002/0051487 A1.

As per claims 1, 5 Stott et al teaches a synchronization system (see figs. 1-2 element 6 and col.4, lines 45-50) in digital communication, comprising: an "A/D" converter is the same as the claimed (converter for receiving signals from a transmitter, and over-sampling a single symbol interval into a plurality of sub-samples (see fig.2 element 20 and col.5, lines 5, lines 18-20); a signal processor for classifying each symbol over-sampled by the converter into a sub-sample group according to a sample phase (see fig.2 elements 22-24 and abstract and col.5, lines 25-40), and performing signal processing to adjust processing speeds (see col.6, lines 6-7); an integrator (see col.11, lines 45-55) for removing noise from the signals output by the signal processor and performing integration during a predetermined time.

However Stott et al does not teach a timing selector for selecting an optimal symbol synchronization point from among values output by the integrator, generating a symbol timing signal and outputting it.

Yamada et al teaches a timing selector for selecting an optimal symbol (see figs 18 and 28 element 81) synchronization point from among values output by the adaptive equalizer (which is known in art as to include multiple FIR or IIR filters having the same functionality as the claimed integrator) (see figs. 18 and 28 elements 17, 63), generating a symbol timing signal and outputting it (see page 6, paragraphs [0073-0074] and page 8, [0092]).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Yamada into Stott as to provide a power sum maximum which would define a symbol sync timing as taught by Yamada (see abstract and page 6 [0073]).

As per claim 2, Stott et al teaches, further comprising a digital demodulator (see figs. 1-2 element 6) for receiving the symbol-timing signal from the signal processor generating a demodulation signal, and outputting it. Furthermore implementing the teaching of Stott into Yamada for receiving the timing selector would have been obvious to one skilled in the art as to provide a power sum maximum which would define a symbol sync timing as taught by Yamada (see abstract and page 6 [0073]).

As per claim 3, Stott teaches wherein the signal processor comprises: a sample arranger for classifying the over-sampled signal output by the converter into a sub-sample group according to a sample phase within the symbol (see fig.2 elements 22-24 and abstract and col.5, lines 25-40); and an absolute value calculator (see fig.9 element

82 and col.10, lines 33-34) for converting the sub-sample values output by the sample arranger into absolute values.

As per claim 4, Stott teaches, wherein the signal processor comprises: a sample arranger for classifying the over-sampled signal output by the converter into a sub-sample group according to a sample phase within the symbol (see fig.2 elements 22-24 and abstract and col.5, lines 25-40). Furthermore Stott in combination with the timing selector of Yamada would teach a sign selector for selecting signals having only either sign from among the respective sub-sample values having positive and negative signs the sub-sample values being output by the sample arranger as to provide a power sum maximum which would define a symbol sync timing as taught by Yamada (see abstract and page 6 [0073]).

As per claim 6, Stott et al teaches, generating a digital demodulation signal (see figs. 1-2 element 6). Furthermore implementing the teaching of Stott into Yamada selecting the optimal symbol synchronization point and using the selected signal and outputting it would have been obvious to one skilled in the art as to provide a power sum maximum which would define a symbol sync timing as taught by Yamada (see abstract and page 6 [0073]).

As per claim 7, Stott et al teaches, wherein the signal processing in (b) converts sub-sample values that are output after they are classified into the sub-sample group (see fig.2 elements 22-24 and abstract and col.5, lines 25-40) into absolute values (see fig.9 element 82 and col.10, lines 33-34).

As per claim 8, Stott in combination with the timing selector of Yamada would teach wherein the signal processing in (b) selects signals having an either sign from among sub-sample values having positive and negative signs sub-sample values being output after being classified into the sub-sample group as to provide a power sum maximum which would define a symbol sync timing as taught by Yamada (see abstract and page 6 [0073]).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ariyavisitakul U.S. Patent No 5,809,086.

Gurney et al U.S. Patent No 5,619,542.

Paff U.S. Patent No 5,425057.

Dutkiewicz et al U.S. Patent No 5,629,960.

Nguyen et al U.S. Patent No 6,411,661 B1.

Petrick U.S. Patent 5,712,870.

Belotserkovsky et al U.S. Patent No 6,621,857 B1.

Genossar et al U.S. Patent No 6,643,321 B1.

Hulbert U.S. Patent No 5,920,555.

Gurantz et al U.S. Patent No 5,550,869.

Yangi U.S. Patent 6,278,727 B1.

Li et al U.S. Patent No 5,963,603.

Peyla et al US Pub No 2003/00535550 A1.

Hong et al US Pub No 2001/0007480 A1.

Arambepola US Patent 6,879,646 B2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

12/31/05

EMMANUEL BAYARD
PRIMARY EXAMINER